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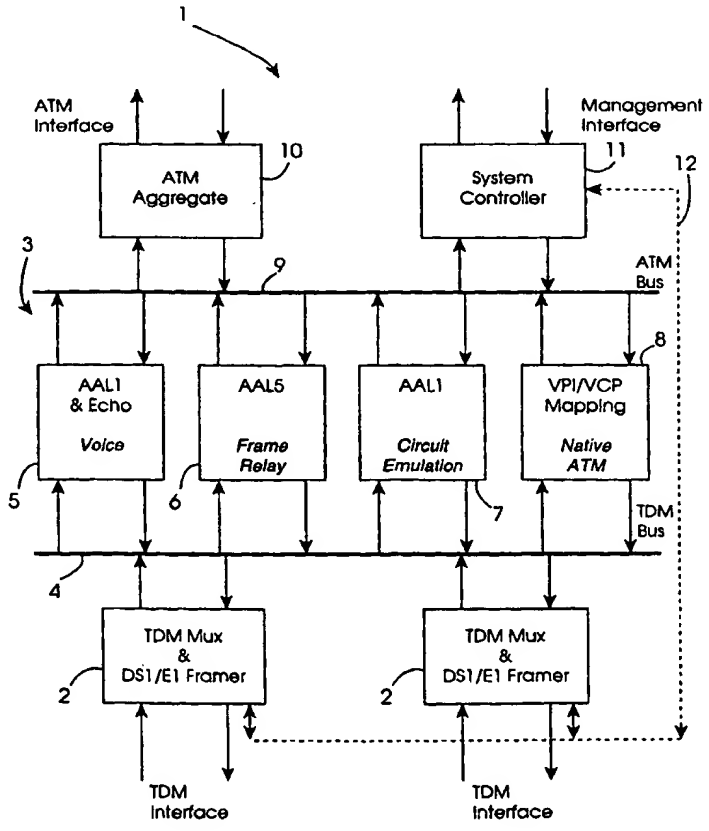
(57) Abstract

A telecommunication system (1) provides bi–directional communication between TDM signals on one side and ATM signals on the other. An ATM aggregate (10) receives and transmits ATM signals, and a TDM interface (2) receives and transmits TDM signals. A format converter has an ATM bus (9) and a TDM bus (4) connected to their respective interfaces. Service–specific adapters (5–8) are connected between the buses.



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"TELECOMMUNICATION SYSTEMS"

INTRODUCTION

Field of the Invention

The invention relates generally to telecommunication systems and more particularly to development of such systems to allow use of different communication formats.

Prior Art Discussion

The most common communication format for telecommunication systems is time division multiplexing (TDM) which is a continuous bit rate service concatenated as multiples of 64 kb/s channels. The TDM technique is particularly effective for voice communication because it is connection-oriented, i.e. a connection link is established initially and is maintained throughout a communication session. Also, the speed and reliability are sufficient for voice.

However, TDM is not particularly effective for data traffic because it is inflexible and does not accommodate the "bursty" nature of data very well. It was for this reason that packet-based techniques have been developed for data communication. For example, the Internet Protocol (IP) technique is used for much Internet service provider (ISP) and local area network (LAN) communication. This technique uses variable-length packets, each of which is independently routed. This means that the technique is not connection-oriented and the bandwidth for a call is not guaranteed for the duration of the call. The general view is that voice subscribers would not tolerate the ensuing unpredictability of call quality. Also, the equipment required for processing to achieve the required speed for voice is quite complex. Therefore, while the IP technique is an approach which may be used to some extent in the future for both voice and data telecommunication networks, problems need to be overcome.

Another packet-based technique is the asynchronous transfer mode (ATM) technique. This has the advantages that it is packet-based and so can handle bursty data traffic well, and is also connection-oriented. In this technique, data is transmitted in fixed-length packets which are typically 53 Bytes in length, having a 48 Byte payload and a 5 Byte header. The header comprises a virtual path identifier (VPI) and a virtual channel identifier (VCI). According to the ATM standard, the cell transfer technique is common to all services and therefore a single ATM stream of cells can include a wide range of different services. Because the cells have a fixed length, timing and control is more predictable. On the other hand, packets in the IP technique are often much longer than ATM cells.

Packet-based techniques are radically different from the TDM technique and therefore it is not practical for a telecommunication operator to change over in a short period of time. In order to introduce packet-based techniques such as ATM, adaptation processes have been developed which are service-specific as different reconstruction techniques are involved. This has led to a large degree of complexity and expense.

It is also known to provide a hybrid system in which TDM and ATM signals are combined in a frame for communication over a link. Such an arrangement is described in PCT Patent Specification No. WO 97/18649 (DSC Communications Corp.). While this arrangement is suitable for specific application areas such as provision of services to a home, it does not appear to be efficient enough for telecommunication networks. This is particularly the case if a number of different services are involved.

European Patent Specification No. EP614324 (Nippon) describes a system for separate TDM/ATM and ATM/TDM conversion. However, this system appears to be quite complex and to be difficult to scale up for increased transaction volume capacity.

Objects of the Invention

The invention is therefore directed towards providing a telecommunication system to allow simpler growth in packet-based technologies in a telecommunication network.

In this specification, the term "packet" is intended to mean both variable-length packets and fixed-length packets (cells). Also, in the remainder of the specification, the term "data" is intended to cover all services, including voice.

SUMMARY OF THE INVENTION

According to the invention, there is provided a telecommunication system comprising:-

a system TDM interface comprising means for receiving and transmitting TDM data streams;

a system packet communication interface comprising means for receiving and transmitting data packet streams; and

a format converter comprising means for performing bi-directional conversion between the interfaces.

By providing bi-directional conversion, the invention allows conversion of telecommunication systems to technologies such as ATM in a gradual manner. Of course, it also allows interfacing of packet-based systems with TDM systems.

In one embodiment, the format converter comprises a TDM bus connected to the TDM interface, a packet bus connected to the packet communication interface, and a conversion means connected between the two buses. Use of buses in this manner

allows a great deal of flexibility in configuration of the conversion means, both in relation to services and hardware and software functionality.

Preferably, the conversion means comprises at least one service-specific adaptation module. Such modules operate efficiently for their particular service, and this arrangement also allows modularity on a service basis.

In one embodiment, the system further comprises a system controller comprising means for controlling operation of circuits in the system. This allows centralised general control. Preferably, the system controller is connected to the packet bus. This allows utilisation of the packet bus for control signals, thus allowing very effective distribution of control signals in a simple manner.

In one embodiment, the system controller comprises means for transmitting and receiving system control signals via the packet bus to the packet communication interface and the format converter, and means for transmitting and receiving system control signals to the TDM interface via a separate TDM control signal link. Thus, conventional-format control signals are used for the TDM circuits.

In one embodiment, the control signals comprise cells such as ATM cells.

Preferably, the system packet communication interface and the format converter comprise means for adding an additional header to each cell to direct routing of the cells within the system. This is a simple and effective way of efficiently distributing cells within the system. For example, the additional header may correlate a virtual circuit with an adaptation module.

In one embodiment, each adaptation module comprises a cell processor connected to an adaptation circuit. By using a cell processor, there is flexibility in the range of cell-processing operations which may be performed.

In another embodiment, each adaptation module further comprises a control processor, and the cell processor comprises means for routing control signal cells to the control processor. By separating control and cell processing, the configuration is simple and easily controlled.

The cell processor routing means may comprise a segmentation and reassembly interface connected to a separate segmentation and reassembly circuit, which is in turn connected to the control processor.

Ideally, the cell processor comprises means for stripping additional headers from cells as they are routed to the segmentation and reassembly circuit.

In one embodiment, the cell processor comprises means for maintaining a plurality of output queues for routing of cells to the TDM bus, the queues being maintained on a priority scheme according to VPI/VCI headers. This allows excellent flexibility in traffic management.

Preferably, each cell processor comprises a mapping function for addition of the additional headers.

Ideally, the cell processor comprises a dedicated ASIC. This allows very efficient cell processing, and also modular construction of the system at a lower level than the system interface and adaptation functions. For example, the system packet communication interface may comprise a cell processor and a bus interface, and the cell processor of the
interface may comprise a similar configuration to the cell processor of each adaptation module.

In one embodiment, the system packet communication interface further comprises a control processor, and the cell processor comprises means for routing control signal cells to the control processor.

According to another aspect, the invention provides a telecommunication system comprising:-

a TDM interface comprising means for receiving and transmitting TDM data streams;

an ATM interface comprising means for receiving and transmitting ATM data streams;

a format converter comprising a TDM bus connected to the TDM interface, an ATM bus connected to the ATM interface, and at least one service-specific adaptation module connected between the buses; and

a system controller.

In one embodiment, the system controller is connected to the ATM bus and comprises means for communicating with the ATM interface and each adaptation module using cells.

In one embodiment, each adaptation module and the ATM interface comprise means for routing control signal cells with additional headers for internal routing.

DETAILED DESCRIPTION OF THE INVENTION

Brief Description of the Drawings

The invention will be more clearly understood from the following description of some embodiments thereof, given by way of example only with reference to the accompanying drawings, in which:-

Figs. 1(a) and 1(b) are overview schematic representations of a telecommunication system of the invention;

Fig. 2 is a diagram illustrating construction of an adaptation module of the system;

Fig. 3 is a diagram illustrating a system ATM interface of the system; and

Fig. 4 is a diagram illustrating an ASIC of the system.

Description of Embodiments

Referring to the drawings, there is illustrated a telecommunication system 1. The purpose of the system 1 is to provide bi-directional conversion between TDM signals on one side and packet-based signals on the other. In this embodiment, the packet-based signals are ATM signals. Conversion is provided in a comprehensive manner whereby a wide variety of different services may be incorporated in the incoming ATM or TDM signals.

Figs. 1(a) and 1(b) show overviews of the system 1. Referring initially to Fig. 1(a), the system 1 is shown at a high level. A bi-directional TDM interface interfaces with external systems in the TDM network and a bi-directional ATM interface interfaces with external systems in the ATM network. Within the system 1, TDM signals are delivered onto, and retrieved from, a TDM bus 4 and ATM signals are delivered onto and retrieved from an ATM bus 9. The buses are part of a format converter which also comprises multiple format conversion units connected between them.

Fig. 1(a) illustrates an important aspect of the invention which is the fact that the TDM and ATM interfaces each communicate their relevant signals within the system via a bus. This allows flexibility in configuration of the format converter as any desired number and type of format conversion units may be connected between

the TDM and ATM buses. These units may be service-specific. Therefore an important aspect of the invention is that the format conversion flexibility applies to allocation of services and also to allocation of circuits within the system for service and hardware utilisation flexibility.

In more detail, and referring to Fig. 1(b), the system 1 comprises in this embodiment three TDM interface units 2 operating at 45 Mb/s. Only two are illustrated, for clarity. The interface units 2 are programmed to demultiplex received TDM signals and to multiplex outgoing TDM signals. Differentiation of services in the signals is achieved by recognition of framing patterns.

The format converter is indicated by the numeral 3 and comprises a TDM bus 4, adaptation modules 5 to 8, and an ATM bus 9. Thus the format conversion units are service-specific adaptation modules, namely voice 5, frame relay 6, circuit emulation 7, and native ATM 8 adaptation modules. Each adaptation module is programmed to extract the relevant incoming TDM or ATM signal for its service, to convert the signal, and to route the converted signal onto the opposite bus for output at the relevant interface. In this embodiment, one module per service is used, however, the flexibility allowed by the architecture allows multiple modules per service

The ATM interface comprises an ATM aggregate 10 operating at 155 Mb/s.

The manner in which the adaptation modules extract the relevant signals is according to control signals from a system controller 11. The controller 11 directs control signals via the ATM bus 9 for the ATM aggregate 10 and for the adaptation modules. The communication protocol is ATM, with specific internal headers. This has been found to be a particularly convenient form of communication. The controller 11 communicates with the TDM interfaces via a separate dedicated link 12 because the latter does not have access to ATM signals.

Referring now to Fig. 2, construction of an individual adaptation module is illustrated, in this case the voice adaptation module 5. The module 5 comprises an ASIC cell processor 20 having inter alia a routing function 21 and a mapping function 22. There is an ATM bus interface 25 connecting it to the ATM bus 9. On the other side, the module 5 is connected via a TDM/ATM adaptation device 26 and a TDM bus interface 27 to the TDM bus 4. For internal control, the module 5 comprises a Segmentation and Reassembly device (SAR) 28 connected to the cell processor 20 and on the other side to a control processor 29. The control processor 29 is connected by a control bus 30 to the SAR 28, the cell processor 20, the adaptation circuit 26, and to the TDM bus interface 27.

As illustrated in Fig. 3 the ATM aggregate 10 has the configuration of an ATM bus interface 40 (connected to the ATM bus 9), a cell processor 41, a SAR 42, and a control processor 43. This configuration may be regarded as a general modular circuit for the system as it forms part of each of the modules 5 to 8. Within the cell processor 41, there is a mapping function 44 and a routing function 45. The latter maintains control signal queues CSQ and traffic queues TQ.

In operation, when a cell is received at the ATM aggregate 10, the VPI/VCI is used by the mapping function 44 in the cell processor 41 to determine the relevant circuit. The mapping function 44 adds an additional 4 Byte header accordingly. This header allows the relevant adaptation module ATM bus interface 25 to extract the cell and pass it to the routing function 21 of the associated cell processor 20. Where there are a number of adaptation modules for each service the additional header specifies the particular ATM bus interface 25 by correlation of the virtual circuit with a physical circuit. This is important for internal traffic management.

The system controller 11 also transmits cells, namely control signal cells to the ATM bus 9. Again, an additional header is used for routing. The routing function reads the additional header 21 to determine whether each cell is part of a control signal or is a traffic cell. If part of a control signal, it strips off the additional header and writes

the remainder (in conventional 53 Byte format) to an output control signal queue (CSQ). Thus, the SAR 28 only handles conventional-format cells, which it converts to messages recognised by the control processor 29. The control processor 29 acts upon these signals to transmit bus control signals to the various parts of the adaptation module. For example, it may set the manner in which the TDM bus interface 27 extracts TDM signals from the TDM bus 4. The control processor 29 transmits responses such as set-up verification signals, failure condition information etc. to the system controller 11 via the SAR 28 and the mapping function 22. This allows the system controller to monitor status of the system 1.

If a received cell is part of the system traffic, the additional 4-Byte header is again stripped off, but the remaining cell is placed in a relevant traffic queue (TQ). The particular queue is chosen according to the VPI/VCI and the additional header to take account of criteria such as service priority. The cells are converted by the adaptation circuit 26, which is pre-configured for and specific to the particular service. The TDM bus interface 4 in turn places the TDM signals on the TDM bus 4.

In the other direction, the manner in which TDM signals are extracted is controlled by the control processor 29 according to control signals from the system controller 11. Examples of extraction conditions are timeslots to be extracted or whether echo cancellation is required.

These signals are converted by the adaptation circuit 26, which outputs ATM cells to the mapping function 22. This function has a look-up table which inserts the additional header for system use. They may specify, for example, a particular ATM aggregate 10 if there are several of them.

The output cell is then directed to the ATM bus interface 25 and then onto the ATM bus 9. It will be noted that the incoming cells from the TDM side do not include control signal cells – all being traffic cells. The cells are retrieved by the ATM bus

interface 40 of the ATM aggregate 10, which in turn directs them to the routing function 45. As control signal cells are also received in this manner, the routing function 45 maintains both traffic queues TQ and control signal queues CSQ.

The cell processors 20 and 41 each comprise an ASIC 50, illustrated in Fig. 4. Cell rates of up to 373 K cells per second are handled. Cells from the line (controlled rate flow) are received by a UTOPIA line interface 51, which passes them to a mapping circuit 52 which performs the VPI/VCI mapping. A policing circuit 53 performs usage parameter control (UPC) by which cells are admitted based on programmed rate control limits. Statistics are kept on the number of cells admitted, number of bad cells, number of policed cells, and the number of disabled cells. The cells are then passed to a backplane interface 54 for transfer on, for example to the ATM bus interface 25.

In the other direction, cells are received by the backplane interface 54 and passed for queue control to a queueing circuit 55. This uses a cell RAM controller 56 to store queued cells externally, and an SRAM controller 57 to store queue configuration data. The queues are maintained for the line interface 51, and for a SAR interface 58. Thus, the queueing circuit 55 together with the cell RAM controller 56 and the SRAM controller implement the routing function. As will be appreciated from Figs. 2 to 4, the queueing is primarily uni-directional. In the case of the adaptation modules, the cells from the TDM/ATM adaptation circuit 26 arrive at a controlled rate and queueing is not necessary. However, in the opposite direction, there is less control over the rate of the incoming traffic cells, and control signal cells are also included. In the case of the ATM aggregate 10, there is synchronisation with the ATM line interface 46 and queueing is not necessary. However, in the opposite direction there is less control as varying numbers of adaptation modules operate at full capacity, and of course control signal cells are also included.

A processor interface 59 with a configuration and status circuit 60 allow processor access to, for example, configure the SRAM initially for such things as queue

control. However, most on-going control is performed using ATM cells via the SAR interface 58.

The processor interface 59 may also receive and transmit cells to/from any of the local or remote cell interfaces in the system, and has the additional ability to insert a CRC-10 check sum on cells it transmits and to verify a CRC-10 check sum on cells it receives. This is useful for generating OAM cells and for verifying the validity of OAM cells. The processor interface 59 is also used for gathering statistical information on the number of ATM cells in the system.

It will be appreciated that the invention provides for relatively simple migration of telecommunication networks to ATM transmission. The system has a large degree of flexibility provided by the array of different adaptation modules. This allows multiple services to interwork over high speed transmission paths between two network types by converting each service in an appropriate adaptation function.

The invention is not limited to the embodiments hereinbefore described, but may be varied in construction and detail within the scope of the claims. For example, while the embodiment illustrated has an ATM interface, this may instead be for any packet-based communication technique such as I.P. In this case the bus connected to this interface handles packets. However, it is still preferred that fixed length packets (cells) are used for internal control and data rather than variable-length packets. This is because such packets generally allow more predictable timing of internal signal routing. The packet communication interface would perform conversion between the external variable-length and the internal fixed-length packet environments. For example, a segmentation and reasssembly device may be used.

Claims

1. A telecommunication system comprising:-

a system TDM interface comprising means for receiving and transmitting TDM data streams;

a system packet communication interface comprising means for receiving and transmitting data packet streams; and

a format converter comprising means for performing bi-directional conversion between the interfaces.

2. A system as claimed in claim 1, wherein the format converter comprises a TDM bus connected to the TDM interface and a packet bus connected to the packet communication interface, and a conversion means connected between the two buses.

3. A system as claimed in claim 2, wherein the conversion means comprises at least one service-specific adaptation module.

4. A system as claimed in any preceding claim, wherein the system further comprises a system controller comprising means for controlling operation of circuits in the system.

5. A system as claimed in claim 4, wherein the system controller is connected to the packet bus.

6. A system as claimed in claim 4 or 5, wherein the system controller comprises means for transmitting and receiving system control signal via the packet bus to the packet communication interface and the format converter, and means

for transmitting and receiving system control signals to the TDM interface via a separate TDM control signal link.

7. A system as claimed in claim 6, wherein the control signals are cells such as ATM cells.

8. A system as claimed in claim 7, wherein the system packet communication interface and the format converter comprise means for adding an additional header to each cell to direct routing of the cells within the system.

9. A system as claimed in any of claims 3 to 8, wherein each adaptation module comprises a cell processor connected to an adaptation circuit.

10. A system as claimed in claim 9, wherein each adaptation module further comprises a control processor, and the cell processor comprises means for routing control signal cells to the control processor.

11. A system as claimed in claim 10, wherein the cell processor routing means comprises a segmentation and reassembly interface connected to a separate segmentation and reassembly circuit, which is in turn connected to the control processor.

12. A system as claimed in claim 11, wherein the cell processor comprises means for stripping additional headers from cells as they are routed to the segmentation and reassembly circuit.

13. A system as claimed in any of claims 9 to 12, wherein the cell processor comprises means for maintaining a plurality of output queues for routing of cells to the TDM bus, the queues being maintained on a priority scheme according to VPI/VCI headers.

14. A system as claimed in claim 13, wherein each cell processor comprises a mapping function for addition of the additional headers

15. A system as claimed in any of claims 9 to 14, wherein the cell processor comprises a dedicated ASIC.

16. A system as claimed in any preceding claim, wherein the system packet communication interface further comprises a control processor, and the cell processor comprises means for routing control signal cells to the control processor.

17. A telecommunication system comprising:-

a TDM interface comprising means for receiving and transmitting TDM data streams;

an ATM interface comprising means for receiving and transmitting ATM data streams;

a format converter comprising a TDM bus connected to the TDM interface, an ATM bus connected to the ATM interface, and at least one service-specific adaptation module connected between the busses; and

a system controller.

18. A system as claimed in claim 17, wherein the system controller is connected to the ATM bus and comprises means for communicating with the ATM interface and each adaptation module using cells.

19. A system as claimed in claim 18, wherein each adaptation module and the ATM interface comprise means for routing control signal cells with additional headers for internal routing.

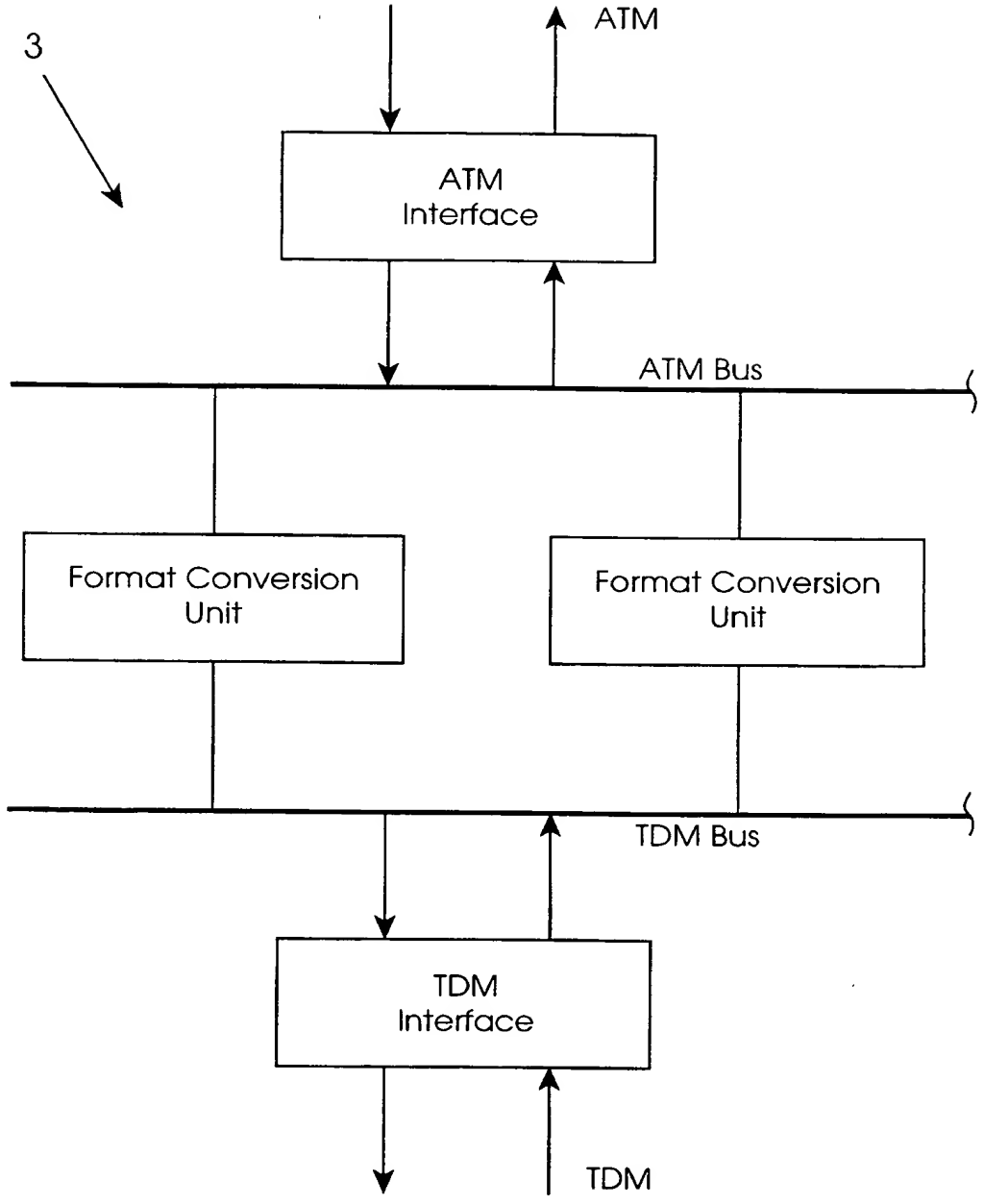
3
ATM
ATM Interface
ATM Bus
Format Conversion Unit
Format Conversion Unit
TDM Bus
TDM Interface
TDM

Fig. 1(a)

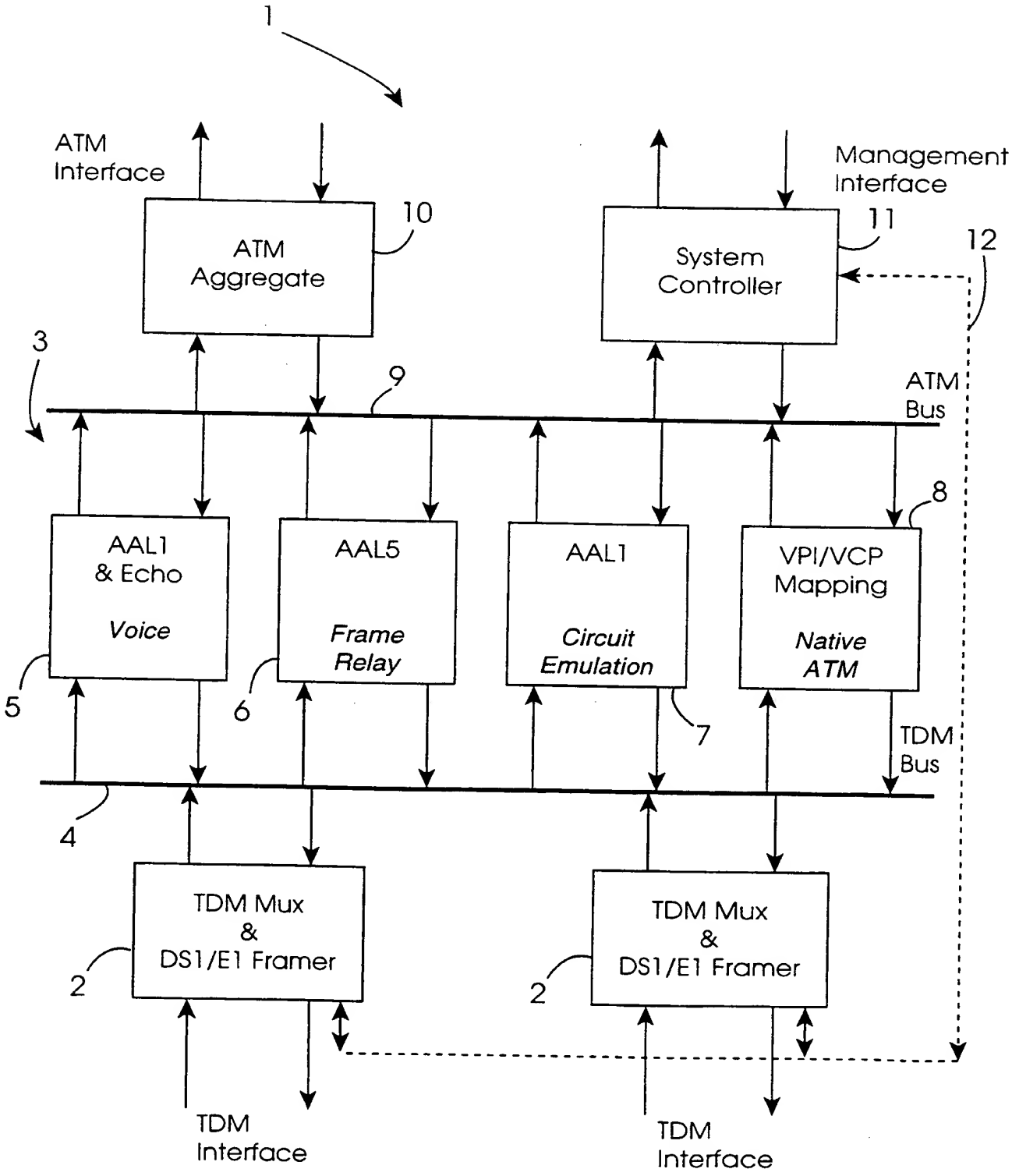
1
ATM Interface
ATM Aggregate
10
Management Interface
System Controller
11
12
3
9
ATM Bus
8
AAL1 & Echo
Voice
AAL5
Frame Relay
AAL1
Circuit Emulation
VPI/VCP Mapping
Native ATM
5
6
7
TDM Bus
4
TDM Mux & DS1/E1 Framer
2
TDM Mux & DS1/E1 Framer
2
TDM Interface
TDM Interface

Fig. 1(b)

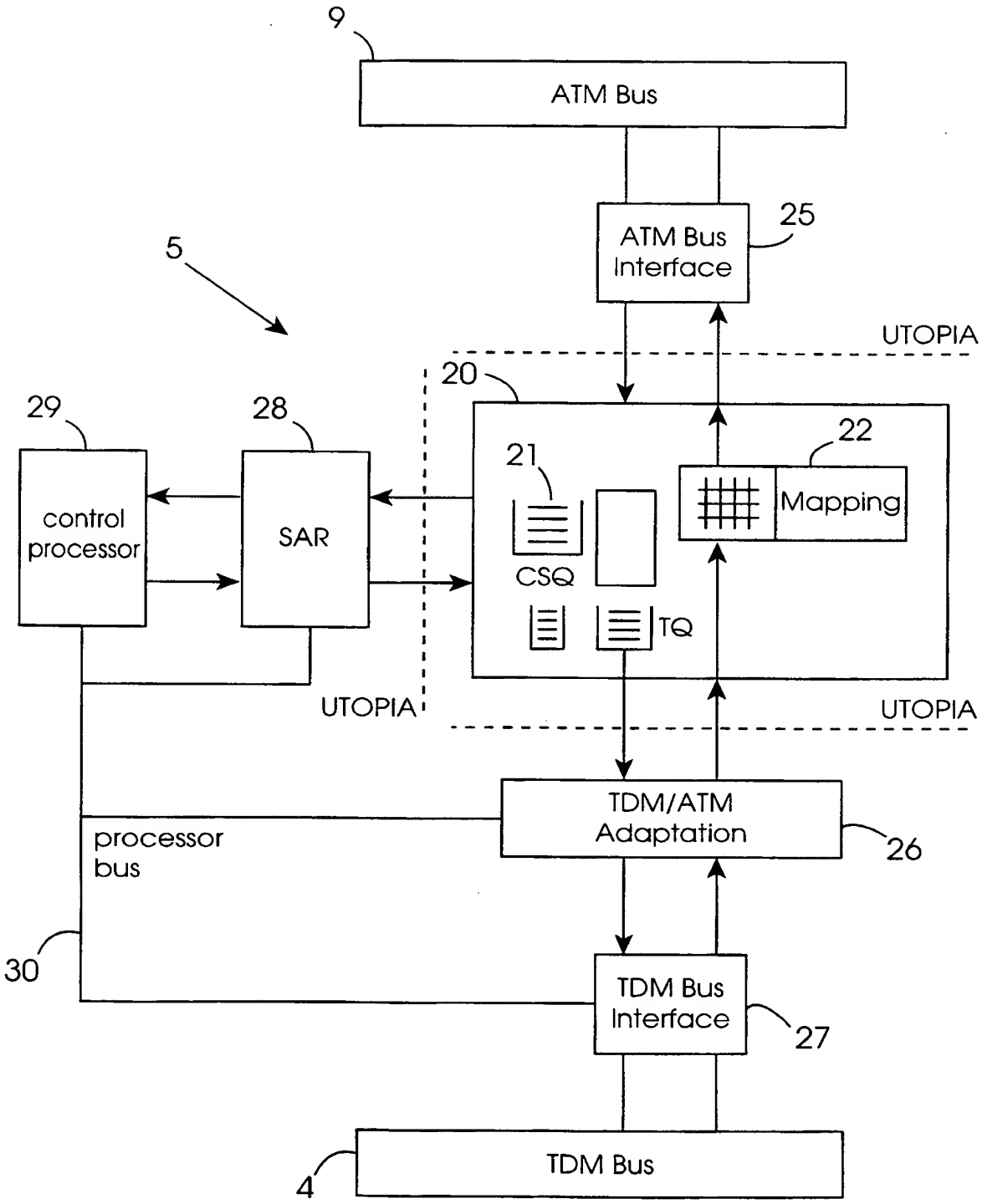
9
ATM Bus
ATM Bus Interface
25
5
UTOPIA
20
29
28
22
21
control processor
SAR
Mapping
CSQ
TQ
UTOPIA
UTOPIA
TDM/ATM Adaptation
26
processor bus
30
TDM Bus Interface
27
4
TDM Bus

Fig. 2

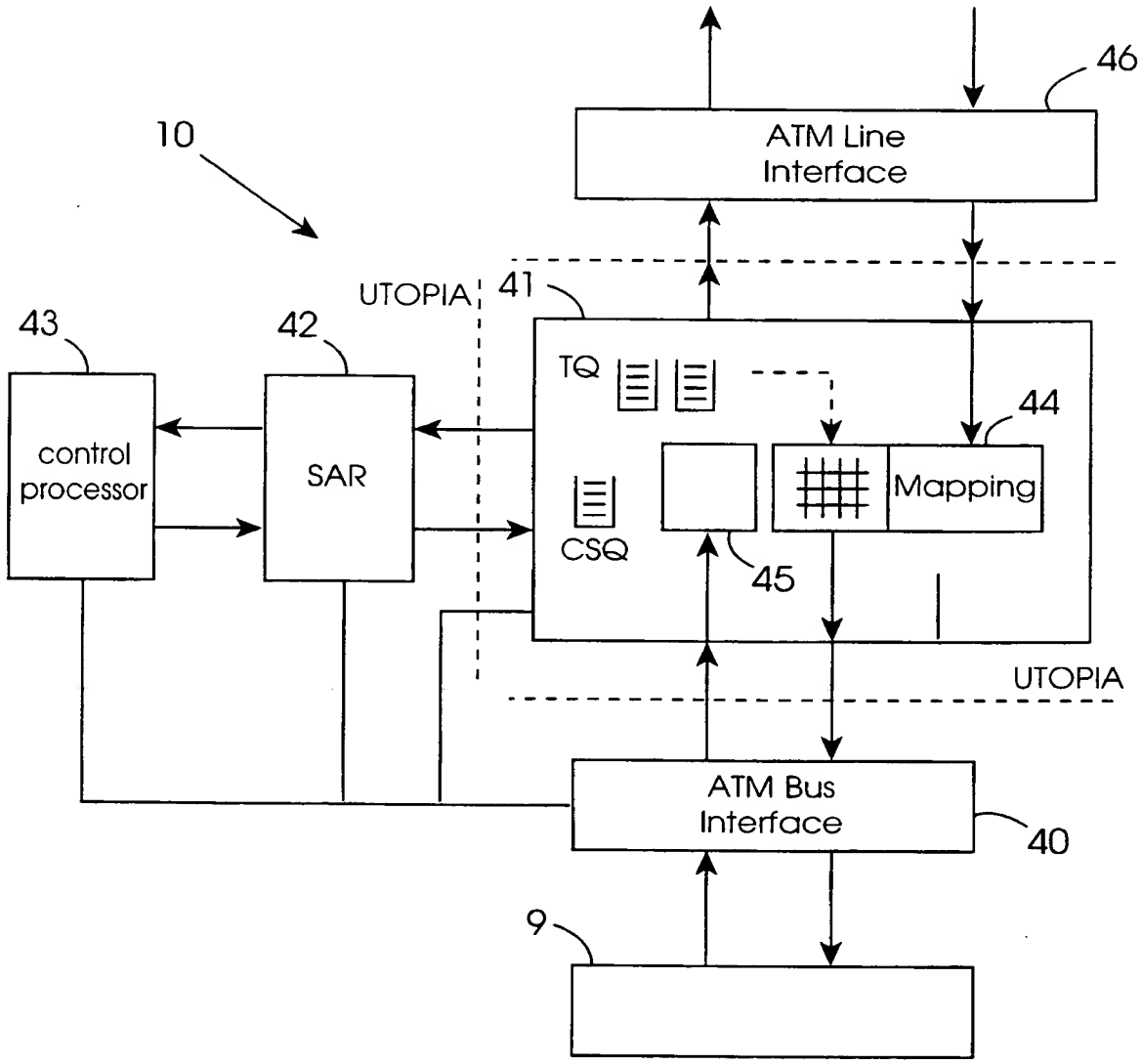
10
46
ATM Line Interface
UTOPIA
41
43
42
TQ
44
control processor
SAR
Mapping
CSQ
45
UTOPIA
ATM Bus Interface
40
9

Fig. 3

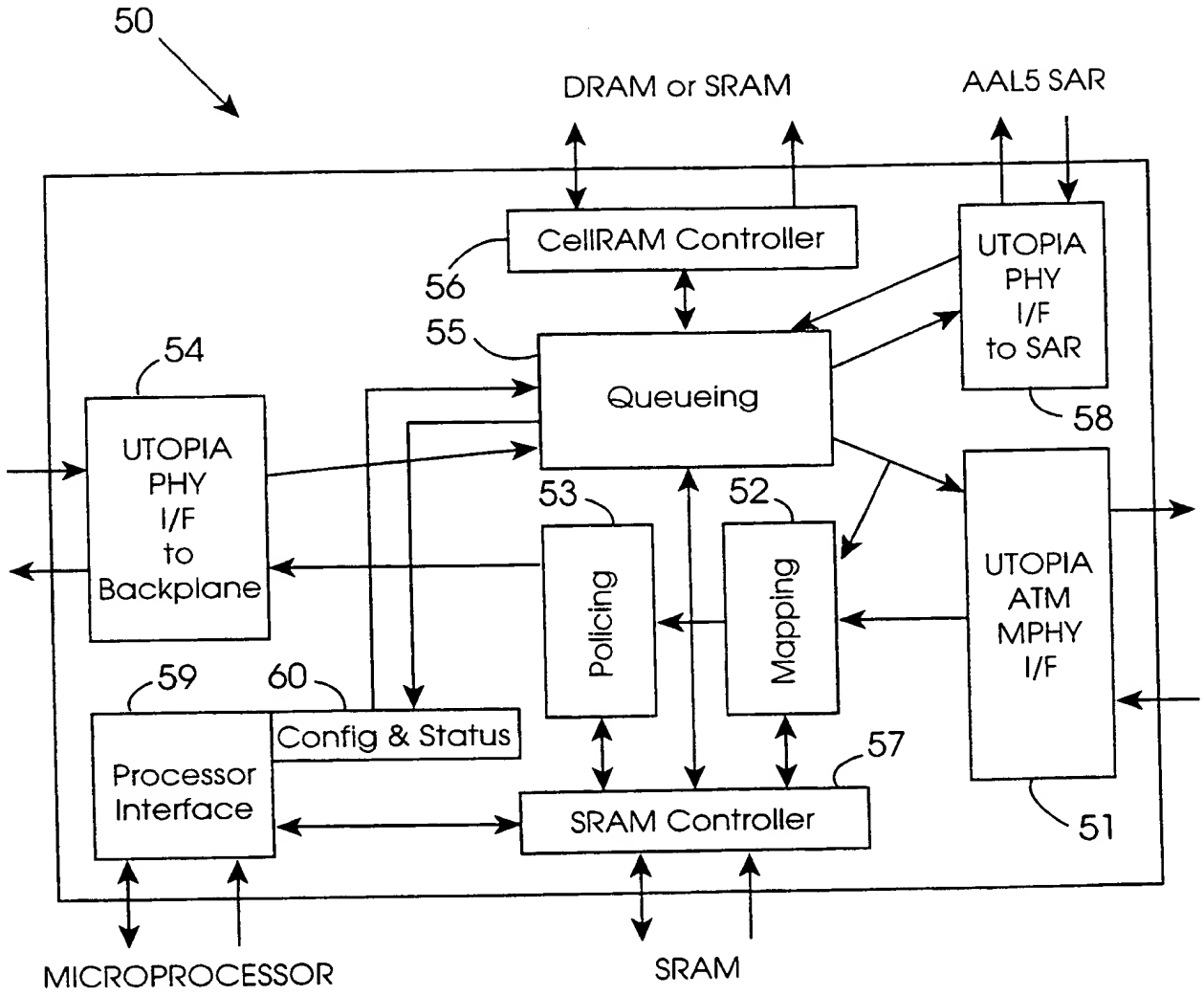
50
DRAM or SRAM
AAL5 SAR
CellRAM Controller
56
55
Queueing
UTOPIA PHY I/F to SAR
58
54
UTOPIA PHY I/F to Backplane
53
52
Policing
Mapping
UTOPIA ATM MPHY I/F
59
60
Config & Status
Processor Interface
57
SRAM Controller
51
MICROPROCESSOR
SRAM

Fig. 4

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INTERNATIONAL SEARCH REPORT

Inter nal Application No
PCT/IE 98/00103

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04Q11/04

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04Q

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 614 324 A (NIPPON ELECTRIC CO) 7 September 1994	1,2,4,5
Y	see column 5, line 54 - column 7, line 36; figures 1,2,9,10 see column 9, line 16 - column 10, line 2 see column 10, line 6 - column 11, line 21 see column 12, line 58 - column 13, line 44	3,9,17
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☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Name and mailing address of the ISA	Authorized officer
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